WHAT IS CLAIMED IS:

1. A semiconductor wafer having a top side and a rear side, the semiconductor wafer comprising:

semiconductor chips arranged in rows and columns on the wafer top side;

strip-type separating regions being arranged between the semiconductor chips; and

wherein the separating regions have passage contacts in the direction of the rear side of the semiconductor wafer.

2. The semiconductor wafer of claim 1, wherein the passage contacts have perforations.

3. The semiconductor wafer of claim 2, wherein the perforations have walls having a metal layer applied thereto.

4. The semiconductor wafer of claim 3, wherein the walls also have an insulation layer applied thereto.

5. The semiconductor wafer of claim 1, wherein the passage contacts have fusible solder material.

6. A semiconductor chip with a top side, a rear side, and with edge sides, the semiconductor chip comprising:

an integrated circuit on the top side;

at least one edge side having edge contacts wherein, the edge contacts extend from the top side in the direction of the rear side of the semiconductor chip; and

wherein the edge contacts are connected to electrodes of the integrated circuit via conductor tracks.

7. The semiconductor chip of claim 5, wherein the edge sides have a perforation-like structure, semicylinder-like cutouts extending as edge contacts from the top side in the direction of the rear side, and have a metal layer.

8. The semiconductor chip of claim 7, wherein the edge sides also have an insulation layer.

9. The semiconductor chip of claim 7, wherein the cutouts have a soldering material.

10. The semiconductor chip of claim 7, wherein the edge contacts are extended on the top side to form a contact area and merge with a conductor track on the top side.

11. The semiconductor chip of claim 7 arranged on a circuit substrate within an electronic component.

12. The semiconductor chip of claim 11, wherein the circuit substrate has a top side and a conductor track structure, the semiconductor chip being arranged with its rear side on the top side of the circuit substrate and the edge contacts being electrically connected to the conductor track structure via contact pads on the top side of the circuit substrate.

13. The semiconductor chip of claim 12, wherein an insulating plastics composition is arranged on the circuit substrate in a manner embedding the edge sides of the semiconductor chip and the contact paths.

14. The semiconductor chip of claim 12, wherein the semiconductor chip is arranged with an edge side on the circuit substrate, the top side of the semiconductor

chip being arranged in angular fashion with respect to the top side of the circuit substrate and the edge contacts being electrically connected to the contact pads.

15. The semiconductor chip of claim 11, wherein a plurality of additional semiconductor chips are stacked one on the other and are electrically connected via the edge contacts among one another and also with respect to external contacts.

16. A method for producing a semiconductor wafer for electronic components, the semiconductor wafer having integrated circuits for semiconductor chips arranged in rows and columns on a wafer top side, with strip-type separating regions between the semiconductor chips, the method comprising:

perforating the semiconductor wafer along the separating regions; and

applying a metal layer to the walls of the perforations.

17. The method of claim 14, wherein the perforations are filled with soldering material before the separation of the semiconductor wafer.